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Claim Amendments

Please amend claims 5 and 16 as follows:

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**Listing of Claims**

1. (previously presented) A method for treating a gate structure comprising a high-K gate dielectric stack to reduce interface states between a high-K gate dielectric and a gate electrode comprising the steps of:

providing a gate dielectric layer stack comprising a high-K gate dielectric over a semiconductor substrate;

forming a gate electrode layer on the gate dielectric layer stack;

lithographically patterning and etching to form a gate structure; and,

carrying out at least one plasma treatment of the gate structure following formation of the gate structure, said at least one plasma treatment comprising a plasma source gas selected from the group consisting of H<sub>2</sub>, N<sub>2</sub>, O<sub>2</sub>, NH<sub>3</sub>, and combinations thereof.

2. (Original) The method of claim 1, further comprising the step

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of annealing the gate structure following the at least one plasma treatment.

3. (Original) The method of claim 2, wherein the step of annealing comprises a temperature of from about 600 °C to about 750 °C.

4. (Original) The method of claim 2, wherein the step of annealing comprises an ambient consisting essentially of nitrogen.

5. (currently amended) The method of claim 1, wherein the gate dielectric layer stack comprises a lowermost SiO<sub>2</sub> layer formed over the ~~silicon~~ semiconductor substrate.

6. (previously presented) The method of claim 1, wherein the gate dielectric layer stack comprises a high-K material selected from the group consisting of tantalum oxides, titanium oxides, hafnium oxides, yttrium oxides, lanthanum oxides, zirconium oxides, and silicates and aluminates thereof.

7. (Original) The method of claim 1, wherein the dielectric layer stack consists essentially of a lowermost SiO<sub>2</sub> layer and an

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overlying hafnium oxide layer.

8. (Original) The method of claim 7, wherein the hafnium oxide layer is formed according to an ALCVD method at a temperature of less than about 300 °C.

9. (previously presented) The method of claim 1, wherein the at least one plasma treatment consists of a plasma source gas selected from the group consisting of hydrogen (H<sub>2</sub>), nitrogen (N<sub>2</sub>), and combinations thereof.

10. (canceled)

11. (Original) The method of claim 1, wherein the plasma treatment is carried out at a pressure of between about 100 mTorr and about 10 Torr.

12. (canceled)

13. (previously presented) A method for treating a gate structure comprising a high-K gate dielectric stack to reduce interface states at a high-K gate dielectric/gate electrode interface comprising the steps of:

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providing a gate dielectric layer stack comprising at least one high-K dielectric over a semiconductor substrate;

forming a gate electrode layer on the high-K dielectric;

lithographically patterning and etching to form a gate structure;

carrying out at least one plasma treatment of the gate structure following formation of the gate structure, said at least one plasma treatment comprising a plasma source gas selected from the group consisting of H<sub>2</sub>, N<sub>2</sub>, O<sub>2</sub>, NH<sub>3</sub>, and combinations thereof; and,

annealing the gate structure following the at least one plasma treatment.

14. (Original) The method of claim 13, wherein the step of annealing comprises a temperature of from about 600 °C to about 750 °C.

15. (previously presented) The method of claim 14, wherein the

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step of annealing comprises an ambient selected from the group consisting of  $H_2$ ,  $N_2$ ,  $O_2$ ,  $NH_3$ , and combinations thereof.

16. (currently amended) The method of claim 13, wherein the gate dielectric layer stack comprises a lowermost  $SiO_2$  layer formed over the ~~silicon~~ semiconductor substrate.

17. (Original) The method of claim 13, wherein the high-K dielectric is selected from the group consisting of tantalum oxides, titanium oxides,, hafnium oxides, yttrium oxides, lanthanum oxides, zirconium oxides, and silicates and aluminates thereof.

18. (Original) The method of claim 13, wherein the gate dielectric layer stack consists essentially of a lowermost  $SiO_2$  layer and an overlying hafnium oxide layer.

19. (previously presented) The method of claim 13, wherein the at least one plasma treatment consists of a plasma source gas selected from the group consisting of hydrogen ( $H_2$ ), nitrogen ( $N_2$ ), and combinations thereof.

20. (Original) The method of claim 13, wherein the plasma

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treatment is carried out at a pressure of between about 100 mTorr and about 5 Torr.

21. (previously presented) A method for treating a gate structure comprising a high-K gate dielectric stack to improve electric performance characteristics comprising the steps of:

providing a high-K gate dielectric layer over a semiconductor substrate;

forming a gate electrode layer on the high-K gate dielectric layer;

patterning said gate electrode layer and gate dielectric layer to form a gate structure; and,

providing a treatment of the gate structure following formation of the gate structure, said treatment selected from the group consisting of a thermal treatment and at least one plasma treatment, said treatment reducing interface states between the gate electrode layer and the high-K gate dielectric layer.

22. (previously presented) The method of claim 21, wherein the

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treatment comprises a plasma treatment followed by the thermal treatment.